引脚定义

PIN DESCRIPTIONS | 2.4英寸 240×320 SPI TFT液晶显示模组

6. PIN DESCRIPTIONS

Pin.No	Symbol	Description
1	GND	Ground
2	RESET	LCM Reset pin
3	SCL	Serial clock pin.
4	RS	Register select pin（Instruction/Data Register Select Pin） RS='1': Display data.（RS=′ 1′ :Select data register） RS='0': Command data.（RS=′ 0′ :Select the instruction register）
5	CS	Chip select pin("Low" enable)
6	SDA	Serial data input
7	SDO	Serial data output.
8	VCC	Power supply for Analog（2.8V-3.3V）
9	LED+	Anode of Backlight
10	LED-	Cathode of Backlight

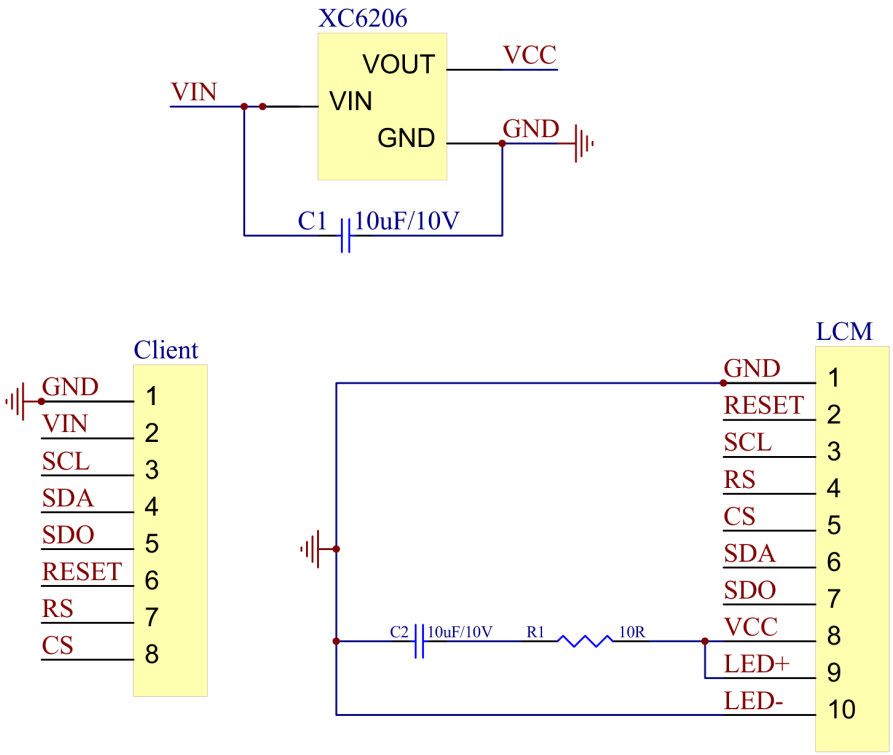
NOTE: The backlight LED can be powered separately or share a set of voltage supply with the VCC.

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接口连接参考图

SCHEMATIC DIAGRAM | 2.4英寸 240×320 SPI TFT液晶显示模组

7. Schematic Diagram

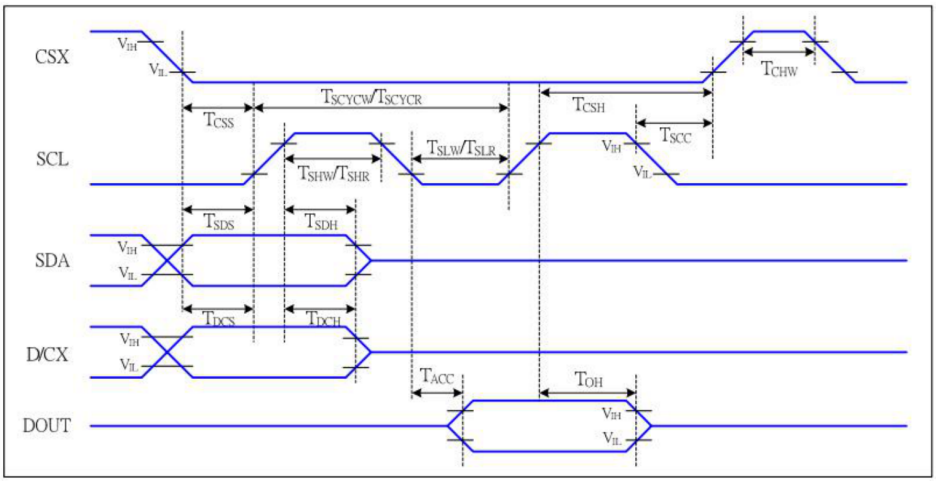


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4线串行接口时序

SERIAL INTERFACE TIMING | 2.4英寸 240×320 SPI TFT液晶显示模组

8. Timing Characteristics



4-line serial Interface Timing Characteristics

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select “H” pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	16		ns	-write command & data ram
	T_{SHW}	SCL “H” pulse width (Write)	7		ns	
	T_{SLW}	SCL “L” pulse width (Write)	7		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	60		ns	
	T_{SLR}	SCL “L” pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	7		ns	
	T_{SDH}	Data hold time	7		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	T_{OH}	Output disable time	15	50	ns	

4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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